SAULT COLLEGE OF APPLIED ARTS & TECHNOLOGY

SAULT STE. MARIE, ONTARIO

COURSE OUTLINE

Course Title: INTERFACING

Course No.: CET302

Program: COMPUTER ENGINEERING TECHNOLOGY

Semester: 6

Date: JANUARY, 1988

Author: TYCHO BLACK

New:_____ Revision: __X__

APPROVED: L P Chazett 88/01/12

Chairperson Date

CET 302

INTERFACING

OBJECTIVES

GENERAL OBJECTIVES

The objectives of this course are to study the general techniques used in computer interfacing, expanding upon the fundamentals learned in CET228, " Microcomputer Circuits and Applications" and to carry out practical exercises with a variety of microcomputer systems. These lab activities will include a Q-BUS interface for a PDP-11 computer, an IBM-PC interface project, an IEEE-488 bus project, and an EPROM programmer exercise. In addition, students will learn to use test equipment such as logic analyzers and signature analyzers in troubleshooting and development.

TEXTBOOK: "MICROCOMPUTER INTERFACING" BY H. STONE

LENGTH OF COURSE: 6 HOURS PER WEEK FOR 1 SEMESTER (16 WEEKS)

METHOD OF ASSESSMENT:

3 WRITTEN THEORY TESTS + Quizzes	60%
LAB PROJECTS	40%

The percentage of assessment for tests and projects may vary slightly from the figures given above.

GRADING SCHEME

COURSE: CET302

1. TESTS

Written tests will be conducted as deemed necessary. They will be announced about one week in advance. Quizzes may be conducted without advance warning.

2. GRADING SCHEME

A+	90	-	100%	Outstanding achievement
A	80	-	89%	Above average achievement
B	70	-	79%	Average Achievement
C	55	-	69%	Satisfactory Achievement

I Incomplete: Course work not complete at Mid-term. Only used at mid-term.

R Repeat

X A temporary grade that is limited to instances where special circumstances have prevented the student from completing objectives by the end of the semester. An X grade must be authorized by the Chairman. It reverts to an R if not upgraded in an agreed-upon time, less than 120 days.

4. UPGRADING OF INCOMPLETES

When a student's course work is incomplete or final grade is below 55%, there is the possibility of upgrading to a pass when the student's performance warrants it. Attendance and assignment completion will have a bearing on whether upgrading will be allowed. A failing grade on all tests will remove the option of any upgrading and an R grade will result. The highest grade on re-written tests or assignments will be 56%.

The method of upgrading is at the discretion of the teacher and may consist of one or more of the following options: assigned make-up work, re-doing projects, re-doing of tests, or writing a comprehensive supplemental examination.

ADDITIONAL REQUIREMENTS:

Completion of the required lab projects is necessary for success in this course. Late submission of reports and poor attendance will have a bearing on final evaluation; generally, a late report will be given a C grade unless extenuating circumstances are involved. The successful completion of a minimum of 4 lab projects is necessary.

Informal lab reports are due one week after completion and will include the following:

LAB REPORT REQUIREMENTS

1. Title page including Title, Date, Lab partner and Project number (#1, 2, 3..5)
2. Statement of the lab's objectives.
3. Brief statement of the procedure.
4. Circuit diagrams properly labelled.
5. Program listings properly documented, data tables, timing diagrams, etc.
6. Where any specific questions have been asked as part of the lab procedure include both the question and the answer.
7. Discussion or Conclusion section in which the results are evaluated, deficiencies are discussed, the degree of completeness is identified, and the important objectives are summarized.

When a lab group works on a project together, a single report showing contributions from both members will be submitted. Where the contribution of one member of a group is seen to be significantly less than another, as would occur for example, when one member is absent from lab sessions, he may not be credited with the lab project and be required to do another in its place.

BLOCK 1: COMPUTER BUSES

At the end of this block the student shall be able to:

1. Describe the nature of a computer bus and its functions.

2. Compare the handshake protocols of synchronous, asynchronous, and semi-synchronous buses.

3. Describe the handshake protocol of the PDP-11 Q-BUS interface circuits, and describe the operation of the DC003, DC004, and DC005 family of interface chips for the QBUS.

4. Describe the operation Q-BUS circuits during given types of cycles or during the processing of an interrupt.

5. Be able to describe the principles of operation and important characteristics of a variety of bus interfaces including the S-100 bus, the STD bus, the MULTIBUS, the UNIBUS, the SCSI Bus, and others as assigned.

BLOCK 2: COMPUTER INTERCONNECTION TECHNIQUES

1. Discuss the need for shielding of computer circuitry, and describe two general rules to follow when interconnecting computers.

2. Discuss possible solutions to the problems of interconnecting devices over relatively long distances.

3. Discuss transmission-line effects in point-to-point connections in computer systems and be able to describe line termination techniques to minimize these effects.

4. List three interconnection methods for point-to-point interconnection of computers, and describe when each might be used, or the advantages and disadvantages of each.

5. Discuss the general characteristics of bus drivers and receivers.

6. Describe the two methods of improving grounding and reducing cross-talk in flat cable.

BLOCK 3: MEMORY SYSTEMS AND DMA

At the end of this block the student shall be able to:

1. Given circuit diagrams, describe the operation and organization of the memory system in an IBM-PC.
2. Discuss the general operation of a DMA controller.
3. Describe the operation of the 8237A DMA Controller in an IBM-PC.
4. Describe the DMA protocol used in the PDP-11 system.
5. Given circuit diagrams, describe the operation of a PDP-11 Q-BUS DMA interface.

BLOCK 4: PARALLEL INTERFACING AND THE IEEE-488 BUS

At the end of this block the student shall be able to:

1. Describe the IEEE-488 bus signals, and the protocol used to transfer information on this bus.
2. Describe the operation and programming requirements of various interface chips for the IEEE-488 bus such as the Intel 8291 and the Motorola 68488.
3. Describe the operation of the IBV11 IEEE-488 bus interface for the PDP-11.
4. Write programs in MACRO-11, FORTRAN or BASIC to control the operation of frequency counters, digital multimeters, and frequency synthesizers using the IEEE-488 bus in an ATE system.

BLOCK 5 MAGNETIC RECORDING

At the end of this block the student shall be able to:

1. Describe the operation and use of phase-locked loops in digital recording.
2. Discuss the various methods of encoding digital information magnetically on disks and tapes.
3. Discuss the problem of data recovery when reading data from disk.
4. Given circuit diagrams, describe the operation of a floppy disk interface, and a floppy disk drive.
5. Describe the operation and programming of a typical floppy disk controller chip.
6. Discuss the operation of, and write programs to control, PDP-11 magnetic tape drives.

BLOCK 6 DISPLAY TECHNIQUES

At the end of this block the student shall be able to:

1. Describe the methods of displaying data on colour and black and white raster-scan CRTs.
2. Describe the typical components of a CRT display interface.
3. Describe the operation of the MC6845 CRT controller chip and its application in typical systems such as the IBM-PC.
4. Given circuit diagrams, describe the operation of the D2 kit CRT controller board.
5. Write programs to initialize the CRT controller and display data on the CRT.
6. Describe the operation of the MC6847 colour video display controller.
7. Describe the features of various graphics adapter standards in use in personal computer systems.

BLOCK 7 INTERFACE SOFTWARE

At the end of this block the student shall be able to:

1. Discuss the use of device drivers in the RT11 and RSX11 operating systems.
2. Describe the operation of a typical device driver for a device such as a terminal or floppy disk controller.
3. Describe the requirements of a device driver, and the steps required to write one.